Notice of Allowability	Application No. 10/082,449	Applicant(s) LI ET AL.	
	Examiner John Pezzlo	Art Unit 2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 10 May 2002*.

2. ☒ The allowed claim(s) is/are *24-49 (renumbered1-26)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/15/2005, 2/23/02
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOHN PEZZLO
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

Claims 24-49 are allowable over the prior art of record.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: The applicants have claimed the following uniquely distinct features in the instant invention, which are not found in the prior art, either singularly or in combination.

1. Regarding claim 24 - A switching fabric comprising N/D PxM input nodes having output ports, M/D NxQ output nodes having input ports, and an interstage exchange interconnecting each one of the input nodes to each one of the output nodes with D lines, each of the lines interconnecting a distinct one of the output ports and a distinct one of the input ports, where D > 1, and D is a common factor of M and N.

2. Regarding claim 31 - A switching network constructed from recursive 2-stage construction, one of the recursive steps constructing a modified 2-stage interconnection network, the modified 2-stage interconnection network comprising N/D PxM input nodes having output ports, M/D NxQ output nodes having input ports, and an interstage exchange interconnecting each one of the input nodes to each one of the output nodes with D lines, each of the lines

interconnecting a distinct one of the output ports and a distinct one of the input ports, where D > 1, and D is a common factor of M and N.

3. Regarding claim 38 - A switch based upon a plurality of opto-electrical-physical implementation levels comprising N/D first switching elements, each having P input ports and M output ports and having a configuration based on a first one of the implementation levels, M/D second switching elements, each having N input ports and Q output ports and having a configuration based on a second one of the implementation levels, and an interface circuit, which is compatible with both the first implementation level and the second implementation level, interconnecting each of the first switching elements to each of the second switching elements with D lines, each line interconnecting a distinct one of the output ports of the first switching elements and a distinct one of the input ports of the second switching elements, where D > 1, and D is a common factor of M and N.

4. Regarding claim 45 - A switch comprising NJD first switching elements arranged as a first stack of NJD parallel planes, each having P input ports and M output ports, M/D second switching elements arranged as a second stack of M/D parallel planes orthogonal to the first stack of planes, each having N input ports and Q output ports, where D > 1. and D is a common factor of M and N, a plurality of first adaptors, wherein every D output ports of each one of the N/D first switching elements are adapted by a first adaptor into a single bundle of D output ports such that each one of the first switching elements has M/D bundles of D output ports, and a plurality of second adaptors, wherein every D input ports of each one of the M/D second switching elements are adapted by a second adaptor into a single bundle of D input ports such that each one of the second switching elements has N/D bundles of D input ports. and wherein

each one of the first switching elements is connected to each one of the second switching elements by the connection of a distinct one of the M/D bundles of output ports and a distinct one of the N/D bundles of input ports.

5. Regarding claim 46 - A method for routing a packet through a $2^{n-d}x2^{n-d}$ k-stage bit-permuting network constructed from modified 2-stage interconnection, the packet having a destination address expressed as $D_1D_2....D_{n-d}$, the network including 2^{r-d} 2^{n-r} $x2^{n-r}$ input nodes, 2^{n-r-d} $2^r x2^r$ output nodes, and an interstage exchange induced by a permutation π on integers from 1 to n-d such that the images of the numbers r-d+1, r-d+2, .. . , n-d cover the numbers 1, 2, . . ., n-r-d, or equivalently, the images of the numbers 1, 2, . . ., r-d are covered by the numbers n-r-d+l, n-r-d+2, ..., n-d, for $1<r<n$ and $l\leq d<\min(r, n-r)$, $k>n-d$, the method comprising generating a routing tag for the packet from the destination address $D_1D_2...D_{n-d}$ and the guide of the network expressed as $\gamma(1), \gamma(2), . . ., \gamma(k)$, the routing tag being a k-symbol string $D_{\gamma(1)}D_{\gamma(2)}.. .D_{\gamma(k)}$, and routing the packet at the j-th stage using $D_{\gamma(1)}$ in the routing tag; $l\leq j\leq k$.

6. Regarding claim 48 - A method for routing a packet through a $2^{n-d}x2^{n-d}$ k-stage bit-permuting network constructed from modified 2-stage interconnection, the packet having a rectangular set of destination addresses expressed as $Q_1Q_2. . .Q_{n-d}$, the network including 2^{r-d} 2^{n-r} $x2^{n-r}$ input nodes, 2^{n-r-d} $2^r x2^r$ output nodes, and an interstage exchange induced by a permutation π on integers from 1 to n-d such that the images of the numbers r-d+1, r-d+2, . . ., n-d cover the numbers 1, 2, ..., n-r-d, or equivalently, the images of the numbers 1, 2, ..., r-d are covered by the numbers n-r-d+l, n-r-d+2, . . ., n-d, for $1<r<n$ and $l\leq d<\min(r, n-r)$, $k>n-d$, the method comprising generating a routing tag for the packet from the rectangular set of destination addresses $Q_1Q_2. . .Q_{n-d}$ and the guide of the network expressed as γ (l), γ (2), . . ., γ (k), the routing tag being a k-

symbol string $Q_{\gamma(1)}Q_{\gamma(2)}..Q_{\gamma(k)}$, whenever $\gamma(p) = \gamma(q)$ in the guide of the network, where $p<q$, disabling the bicasting function of the whole stage of switching nodes at either stage-p or stage-q, and routing the packet at the j-th stage using $Q_{\gamma(j)}$ in the routing tag, $1 \leq j \leq k$.

7. Regarding claim 49 - A method for constructing a switch based upon a plurality of opto-electrical-physical implementation levels, the method comprising configuring N/D first switching elements based on a first one of the implementation levels, each of the first switching elements having P input ports and M output ports, configuring M/D second switching elements based on a second one of the implementation levels, each of the second switching elements having N input ports and Q output ports, and configuring an interface circuit, which is compatible with both the first implementation level and the second implementation level, to realize the interconnection between the first switching elements and the second switching elements such that each of the first switching elements is connected to each of the second switching elements with D lines, each line interconnecting a distinct one of the output ports of the first switching elements and a distinct one of the input ports of the second switching elements, where $D > 1$, and D is a common factor of M and N.

The closest prior art, either singularly or in combination, fail to anticipate or render the above limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Claims 24-49 being allowable, **Prosecution On The Merits Is Closed** in this application.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Chao (US 5,179,552 A) discloses a crosspoint matrix switching element for a packet switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(571) 273-8300

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

Jefferson Building

500 Dulany Street

Alexandria, VA.

John Pezzlo

7 November 2005

JOHN PEZZLO
PRIMARY EXAMINER